Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **1A**
2. **1Y**
3. **2A**
4. **2Y**
5. **3A**
6. **3Y**
7. **GND**
8. **4Y**
9. **4A**
10. **5Y**
11. **5A**
12. **6Y**
13. **6A**
14. **Vcc**

**.051”**

**2 1 14 13**

**3**

**4**

**5**

**12**

**11**

**10**

**6 7 8 9**

**MASK REF**

**HC04E**

**.053”**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: Vcc (or leave FLOATING)**

**Mask Ref: HC04E**

**APPROVED BY: DK DIE SIZE .051” X .053” DATE: 2/28/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD74HC04**

**DG 10.1.2**

#### Rev B, 7/19/02